Teruo Tanimoto

Associate professor of Faculty at Information Science and Electrical Engineering, Kyushu University

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Education

Apr. 2015 – Mar. 2018	Ph.D. of Engineering. Kyushu University, Fukuoka Advisor: Prof. Koji Inoue
Apr. 2010 - Mar. 2012	Master of Information Science and Technology, The University of Tokyo, Tokyo Advisor: Prof. Hiroshi Nakamura
Apr. 2006 - Mar. 2010	Bachelor of Engineering, The University of Tokyo, Tokyo Advisor: Prof. Hiroshi Nakamura

Work Experience

Apr. 2022 - present	Associate professor at Faculty of Information Science and Electrical Engineering, Kyushu University. (Concurrently visiting researcher at RIKEN center for Quantum Computing)
Apr. 2021 – Mar. 2022	Assistant professor at Faculty of Information Science and Electrical Engineering, Kyushu University. (Concurrently visiting researcher at RIKEN center for Quantum Computing)
Apr. 2018 – Mar. 2021	Assistant professor at Research Institute for Information Technology, Kyushu University. (Concurrently Cybersecurity Center, Kyushu University)
Apr. 2015 – Mar. 2018	Research Assistant at Kyushu University
Apr. 2012 – Mar. 2015	Researcher at Fujitsu Laboratories Limited, Kawasaki, Japan I designed and prototyped both hardware and software for an inter-node communication system for UNIX server products.

Refereed Publications

1. Yosuke Ueno, Yuna Tomida, Teruo Tanimoto, Masamitsu Tanaka, Yutaka Tabuchi, Koji Inoue and Hiroshi Nakamura, “Inter-Temperature Bandwidth Reduction in Cryogenic QAOA Machines,” IEEE Computer Architecture Letters (Early Access), Oct. 2023.
2. Kuan Yi Ng, Aalaa M. A. Babai, Teruo Tanimoto, Satoshi Kawakami and Koji Inoue, “Empirical Power-Performance Analysis of Layer-wise CNN Inference on Single Board Computers,” Journal of Information Processing, Vol.31, pp.478-494, Aug. 2023. (also printed in IPSJ Transactions on Advanced Computer Systems)
3. Yasunari Suzuki, Yosuke Ueno, Wang Liao, Masamitsu Tanaka and Teruo Tanimoto, “Circuit Designs

for Practical-Scale Fault-Tolerant Quantum Computing," In Proceedings of Symposium on VLSI Technology and Circuits (VLSI '23), pp. 1-2, June 2023 (invited).

4. Ikki Nagaoka, Ryota Kashima, Masamitsu Tanaka, Satoshi Kawakami, Teruo Tanimoto, Taro Yamashita, Koji Inoue and Akira Fujimaki, "50-GFLOPS Floating-Point Adder and Multiplier Using Gate-Level-Pipelined Single-Flux-Quantum Logic with Frequency-Increased Clock Distribution," IEEE Transactions on Applied Superconductivity, vol. 33, no. 4, pp. 1-11, June 2023, Art no. 1302711.
5. Wang LIAO, Yasunari Suzuki, Teruo Tanimoto, Yosuke Ueno and Yuuki Tokunaga, "WIT-Greedy: Hardware System Design of Weighted ITerative Greedy Decoder for Surface Code," In Proceedings of the 28th Asia and South Pacific Design Automation Conference (ASP-DAC '23), pp. 209-215, Jan. 2023.
6. Satoshi Matsushita, Teruo Tanimoto, Satoshi Kawakami, Takatsugu Ono and Koji Inoue, "An Edge Autonomous Lamp Control with Camera Feedback," In Proceedings of the IEEE 8th World Forum on Internet of Things (WF-IoT '22), pp. 1-7, Oct.-Nov. 2022.
7. Yasunari Suzuki, Takanori Sugiyama, Tomochika Arai, Wang Liao, Koji Inoue and Teruo Tanimoto, "Q3DE: A fault-tolerant quantum computer architecture for multi-bit burst errors by cosmic rays," In Proceedings of the 55th IEEE/ACM International Symposium on Microarchitecture (MICRO-55), pp. 1110-1125, Oct. 2022.
8. Ilkwon Byun, Junpyo Kim, Dongmoon Min, Ikki Nagaoka, Kosuke Fukumitsu, Iori Ishikawa, Teruo Tanimoto, Masamitsu Tanaka, Koji Inoue and Jangwoo Kim, "XQsim: Modeling Cross-Technology Control Processors for 10+K Qubit Quantum Computers," In Proceedings of ACM/IEEE International Symposium on Computer Architecture (ISCA '22), pp. 366-382, June 2022.
9. Iori Ishikawa, Ikki Nagaoka, Ryota Kashima, Koki Ishida, Kosuke Fukumitsu, Keitaro Oka, Masamitsu Tanaka, Satoshi Kawakami, Teruo Tanimoto, Takatsugu Ono, Akira Fujimaki and Koji Inoue, "Design of Variable Bit-Width Arithmetic Unit Using Single Flux Quantum Device," In Proceedings of International Symposium on Circuits & Systems 2022 (ISCAS '22), pp. 3547-3551, May 2022.
10. Koki Ishida, Ilkwon Byun, Ikki Nagaoka, Kousuke Fukumitsu, Masamitsu Tanaka, Satoshi Kawakami, Teruo Tanimoto, Takatsugu Ono, Jangwoo Kim and Koji Inoue, "Superconductor Computing for Neural Networks," IEEE Micro, vol.41, no.3, pp.19–26, May-June 2021.
11. Koki Ishida, Il-Kwon Byun, Ikki Nagaoka, Kosuke Fukumitsu, Masamitsu Tanaka, Satoshi Kawakami, Teruo Tanimoto, Takatsugu Ono, Jangwoo Kim and Koji Inoue, "SuperNPU: Architecting an Extremely Fast Neural Processing Unit Using Superconducting Logic Devices," In Proceedings of the 53rd IEEE/ACM International Symposium on Microarchitecture (MICRO-53), pp. 58-72, Oct. 2020.
12. Koki Ishida, Masamitsu Tanaka, Ikki Nagaoka, Takatsugu Ono, Satoshi Kawakami, Teruo Tanimoto, Akira Fujimaki and Koji Inoue, "32 GHz 6.5 mW Gate-Level-Pipelined 4-bit Processor using Superconductor Single-Flux-Quantum Logic," In Proceedings of the 2020 Symposia on VLSI Technology and Circuits, pp.1-2, June 2020.
13. Keitaro Oka, Satoshi Kawakami, Teruo Tanimoto, Takatsugu Ono and Koji Inoue, "Enhancing a manycore-oriented compressed cache for GPGPU," In Proceedings of the International Conference on High Performance Computing in Asia-Pacific Region (HPCAsia2020), pp.22-31, Jan. 2020.
14. Teruo Tanimoto, Takatsugu Ono and Koji Inoue, "Critical Path based Microarchitectural Bottleneck Analysis for Out-of-Order Execution," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E102-A, No.6, pp.758-766, Jun. 2019.
15. Teruo Tanimoto, Takatsugu Ono and Koji Inoue, "Dependence Graph Model for Accurate Critical Path

Analysis on Out-of-Order Processors," IPSJ Journal of Information Processing, Vol.25, pp.983-992, Dec. 2017. (also printed in IPSJ Transactions on Advanced Computer Systems)

16. Teruo Tanimoto, Takatsugu Ono and Koji Inoue, "CPCI Stack: Metric for Accurate Bottleneck Analysis on OoO Microprocessors," In Proceedings of the Fifth International Symposium on Computing and Networking (CANDAR '17), pp.166-172, Nov. 2017.
17. Hiroshi Sasaki, Fang-Hsiang Su, Teruo Tanimoto and Simha Sethumadhavan, "Why Do Programs Have Heavy Tails?" In Proceedings of the 2017 IEEE International Symposium on Workload Characterization (IISWC '17), pp.135-145, Oct. 2017.
18. Teruo Tanimoto, Takatsugu Ono, Koji, Inoue and Hiroshi Sasaki, “Enhanced Dependence Graph Model for Critical Path Analysis on Modern Out-of-Order Processors,” IEEE Computer Architecture Letters , vol.16, no.2, pp.111-114, July-Dec. 2017.
19. Hiroshi Sasaki, Fang-Hsiang Su, Teruo Tanimoto and Simha Sethumadhavan, ”Heavy Tails in Program Structure,” IEEE Computer Architecture Letters , vol.16, no.1, pp.34-37, Jan.-June 2016.
20. Takatsugu Ono, Yotaro Konishi, Teruo Tanimoto, Noboru Iwamatsu, Takashi Miyoshi and Jun Tanaka, “A Flexible Direct Attached Storage for a Data Intensive Application,” IEICE Transaction on Information and Systems, Vol.E98-D, No.12, pp.2168-2177, Dec. 2015.
21. Takatsugu Ono, Yotaro Konishi, Teruo Tanimoto, Noboru Iwamatsu, Takashi Miyoshi and Jun Tanaka, “FlexDAS: A Flexible Direct Attached Storage for I/O Intensive Applications,” In Proceedings of IEEE International Conference on Big Data (IEEE BigData ‘14), pp.147-152, Oct. 2014.
22. Teruo Tanimoto, Takatsugu Ono, Kohta Nakashima and Takashi Miyoshi, “Hardware-assisted Scalable Flow Control of Shared Receive Queue,” In Proceedings of the 28th ACM International Conference on Supercomputing (ICS ‘14), pp.175-175, Jun. 2014. (poster session)
23. Hiroshi Sasaki, Teruo Tanimoto, Koji Inoue, and Hiroshi Nakamura, “Scalability-based Manycore Partitioning,” In Proceedings of the 21st International Conference on Parallel Architectures and Compilation Techniques (PACT ‘12), pp.107-116, Sep. 2012.

Research Interests

Computer architecture, hardware/software co-design, interconnects, application-specific CPU-FPGA hybrid computing system design, quantum computer system architecture